Code No: 158BH **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech IV Year II Semester Examinations, July - 2023

LOW POWER VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.

ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.

iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) Why the aspect ratio of the device need be larger to minimize short channel effects. [2]

b) Mention the two types of power dissipation in a circuit. [3]

c) How to minimize the switched capacitance? [2]

d) What are the advantages and disadvantages of parallel processing? [3]

e) Mention the advantages of Carry save adder. [2]

f) Draw the full adder circuit and mention its truth table. [3]

g) Delay through 4: 2 compressor is equivalent to how many XOR gate delays. [2]

h) What are the limitations of Braun multiplier? [3]

i) Mention the two types of RAM's. [2]

j) Draw the circuit diagram of one transistor memory cell. [3]

PART – B

(50 Marks)

2.a) Mention various sources of power dissipation and explain them in detail.

b) Explain hallow doping. [5+5]

OR

3.a) Write a brief note on hot electron effect .

b) Explain the concept of direct tunneling. [5+5]

4.a) Explain about the low power design approaches, multiple channel length and multiple body bias.

b) Draw the schematic diagram and explain MTCMOS circuit. [5+5]

OR

5.a) Explain about the dynamic threshold CMOS circuit.

b) Differentiate the system level and circuit level measures for switched capacitance minimization. [6+4]

6.a) Explain the operation of BiCMOS adder circuit.

b) Explain the basic theory and operation of Carry Look Ahead Adder. [5+5]

OR

7.a) Explain the basic theory and operation of carry select adder.

b) What are the advantages of low power, low voltage logic styles? [6+4]

8.a) Explain the operation of Braun Multiplier.

b) List the types of multiplier architectures and explain them briefly. [5+5]

OR

9.a) Discuss the operation of Booth Multiplier.

b) Mention the basic differences between Braun Multiplier and Enhanced Braun Multiplier. [6+4]

10.a) Discuss the future trends and developments of ROM Cells.

b) Draw the architecture of a shared BL SRAM cell and explain it. [5+5]

OR

11.a) Explain the low power techniques at architecture level in ROM design.

b) Explain the architecture and operation of basic DRAM. [5+5]

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